24LC01B/02B MODULES

1K/2K I^2C™ Serial EEPROMs in ISO Micromodules

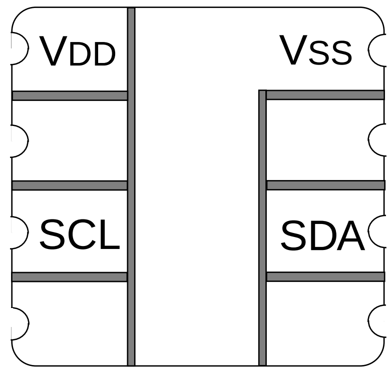
FEATURES

- ISO 7816 Compliant pad locations
- Low power CMOS technology
  - 1 mA active current typical
  - 10 µA standby current typical at 5.5V
- Organized as a single block of 128 bytes (128 x 8) or 256 bytes (256 x 8)
- 2-wire serial interface bus, I^2C™ compatible
- 100 kHz (2.5V) and 400 kHz (5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page-write buffer for up to 8 bytes
- 2 ms typical write cycle time for page-write
- ESD protection > 4 kV
- 1,000,000 E/W cycles guaranteed
- Data retention > 200 years
- Temperature ranges available:
  - Commercial (C): 0°C to +70°C

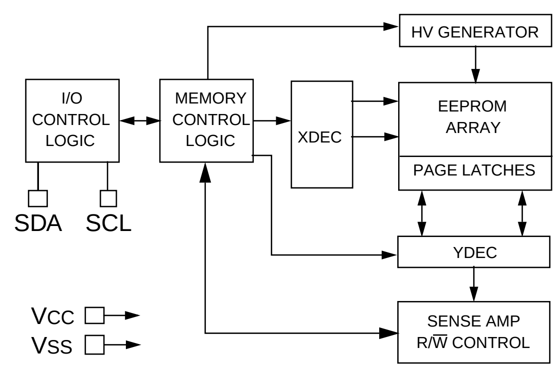
DESCRIPTION

The Microchip Technology Inc. 24LC01B and 24LC02B are 1K-bit and 2K-bit Electrically Erasable PROMs in ISO modules for smart card applications. The devices are organized as a single block of 128 x 8-bit or 256 x 8-bit memory with a two-wire serial interface. The 24LC01B and 24LC02B also have page-write capability for up to 8 bytes of data.

ISO MODULE LAYOUT



BLOCK DIAGRAM



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1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

V_{CC}..7.0V
All inputs and outputs w.r.t. V_{SS} ....-0.6V to V_{CC} +1.0V
Storage temperature .... -65˚C to +150˚C
Ambient temp. with power applied................. -65˚C to +125˚C
ESD protection on all pads...≥4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: PAD FUNCTION TABLE

Name	Function
V_{SS}	Ground
SDA	Serial Address/Data I/O
SCL	Serial Clock
V_{CC}	+2.5V to 5.5V Power Supply

1.2 Pad Descriptions

1.2.1 SDA (Serial Data)

This is a bi-directional pad used to transfer addresses and data into and data out of the device. It is an open drain terminal, therefore the SDA bus requires a pull-up resistor to V_{CC} (typical 10 KΩ for 100 kHz, 2 KΩ for 400 kHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the START and STOP conditions.

1.2.2 SCL (Serial Clock)

This input is used to synchronize the data transfer from and to the device.

TABLE 1-1 DC CHARACTERISTICS

All Parameters apply across the recommended operating ranges unless otherwise noted.	Commercial (C): Tamb = 0˚C to +70˚C, V_{CC} = 2.5V to 5.5V				
Parameter	**Symbol**	**Min.**	**Max.**	**Units**	**Conditions**
SCL and SDA pins:					
High level input voltage	V_{IH}	0.7 V_{CC}		V	(Note)
Low level input voltage	V_{IL}		0.3 V_{CC}	V	(Note)
Hysteresis of Schmitt trigger inputs	V_{HYS}	0.05 V_{CC}	—	V	V_{CC} ≥ 2.5V (Note)
Low level output voltage	V_{OL}		0.40	V	I_{OL} = 3.0 mA, V_{CC} = 4.5V I_{OL} = 2.1 mA, V_{CC} = 2.5V
Input leakage current	I_{LI}	-10	10	µA	V_{IN} = V_{CC} or V_{SS}
Output leakage current	I_{LO}	-10	10	µA	V_{OUT} = V_{CC} or V_{SS}
Pin capacitance (all inputs/outputs)	C_{IN}, C_{OUT}	—	10	pF	V_{CC} = 5.0V (Note) Tamb = 25˚C, f = 1 MHz
Operating current	I_{CC} Write	—	3	mA	V_{CC} = 5.5V, SCL = 400 kHz
	I_{CC} Read	—	1	mA	V_{CC} = 5.5V, SCL = 400 kHz
Standby current	I_{CCS}	—	100	µA	V_{CC} = 5.5V, SDA = SCL = V_{CC}

Note: This parameter is periodically sampled and not 100% tested.

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TABLE 1-2 AC CHARACTERISTICS

All parameters apply across the specified operating ranges unless otherwise noted.	Vcc = 2.5V to 5.5V Commercial (C): Tamb = 0°C to +70°C

Parameter	Symbol	Vcc = 2.5V - 5.5V STD MODE		Vcc = 4.5V - 5.5V FAST MODE		Units	Remarks
		Min.	**Max.**	**Min.**	**Max.**		
Clock frequency	FCLK	—	100	—	400	kHz	
Clock high time	THIGH	4000	—	600	—	ns	
Clock low time	TLOW	4700	—	1300	—	ns	
SDA and SCL rise time	TR	—	1000	—	300	ns	(Note 1)
SDA and SCL fall time	TF	—	300	—	300	ns	(Note 1)
START condition hold time	THD:STA	4000	—	600	—	ns	After this period the first clock pulse is generated
START condition setup time	TSU:STA	4700	—	600	—	ns	Only relevant for repeated START condition
Data input hold time	THD:DAT	0	—	0	—	ns	(Note 2)
Data input setup time	TSU:DAT	250	—	100	—	ns	
STOP condition setup time	TSU:STO	4000	—	600	—	ns	
Output valid from clock	TAA	—	3500	—	900	ns	(Note 2)
Bus free time	TBUF	4700	—	1300	—	ns	Time the bus must be free before a new transmission can start
Output fall time from VIH minimum to VIL maximum	TOF	—	250	20 +0.1 C_B	250	ns	(Note 1), $C_B \leq 100$ pF
Input filter spike suppression (SDA and SCL pins)	TSP	—	50	—	50	ns	(Notes 1, 3)
Write cycle time	TWC	—	10	—	10	ms	Byte or Page mode
Endurance		1M	—	1M	—	cycles	25°C, VCC = 5.0V, Block Mode (Note 4)

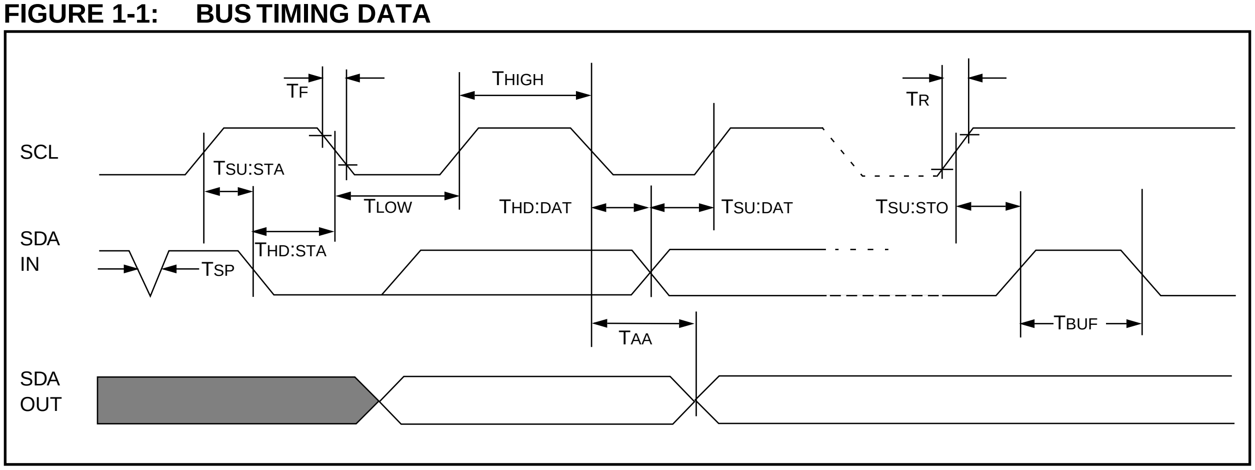
Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

3: The combined TSP and VHYS specifications are due to Schmitt trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but guaranteed by characterization. For endurance estimates in a specific application, please consult the Total Endurance Model which can be obtained on our BBS or website.

FIGURE 1-1: BUS TIMING DATA



2.0 FUNCTIONAL DESCRIPTION

The 24LC01B/02B supports a bi-directional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions, while the 24LC01B/02B works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following bus protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as a START or STOP condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain HIGH.

3.2 Start Data Transfer (B)

A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition.

3.3 Stop Data Transfer (C)

A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and STOP conditions is determined by the master device and is theoretically unlimited, although only the last 16 will be stored when doing a write operation. When an overwrite does occur, it will replace data in a first in first out fashion.

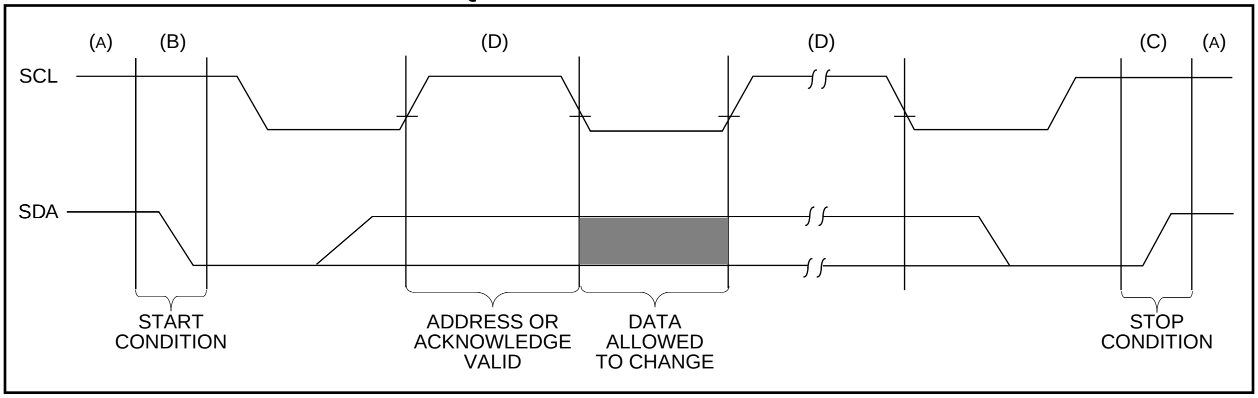
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit.

Note:	The 24LC01B/02B does not generate any acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



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4.0 BUS CHARACTERISTICS

4.1 Slave Address

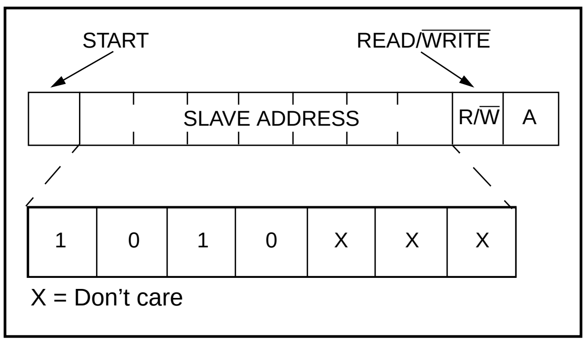
After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the 24LC01B/02B, followed by three don't care bits.

The eighth bit of slave address determines if the master device wants to read or write to the 24LC01B/02B (Figure 4-1).

The 24LC01B/02B monitors the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true, and it is not in a programming mode.

Operation	Control Code	Chip Select	R/$\overline{W}$
Read	1010	XXX	1
Write	1010	XXX	0

FIGURE 4-1: CONTROL BYTE ALLOCATION



5.0 WRITE OPERATION

5.1 Byte Write

Following the start signal from the master, the device code (4 bits), the don't care bits (3 bits), and the R/$\overline{W}$ bit, which is a logic low, is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the address pointer of the 24LC01B/02B. After receiving another acknowledge signal from the 24LC01B/02B, the master device will transmit the data word to be written into the addressed memory location. The 24LC01B/02B acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this time the 24LC01B/02B will not generate acknowledge signals (Figure 5-1).

5.2 Page Write

The write control byte, word address, and the first data byte are transmitted to the 24LC01B/02B in the same way as in a byte write. But instead of generating a stop condition, the master transmits up to eight data bytes to the 24LC01B/02B, which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each word, the three lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than eight words prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin (Figure 5-2).

FIGURE 5-1: BYTE WRITE

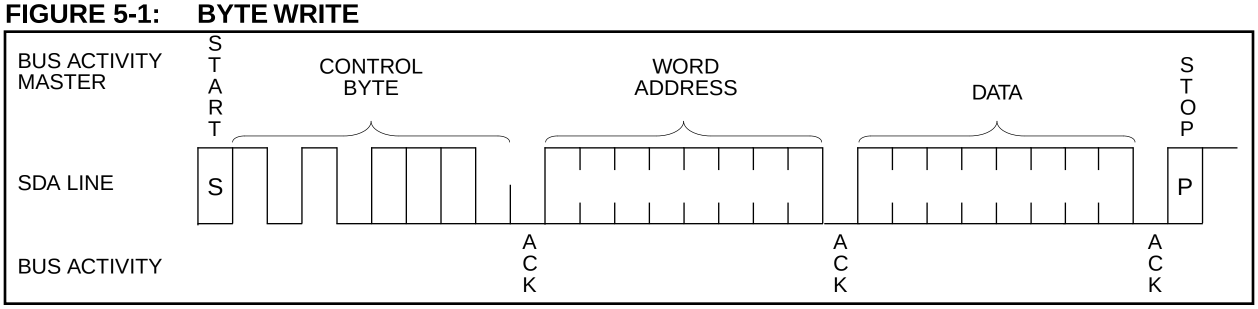
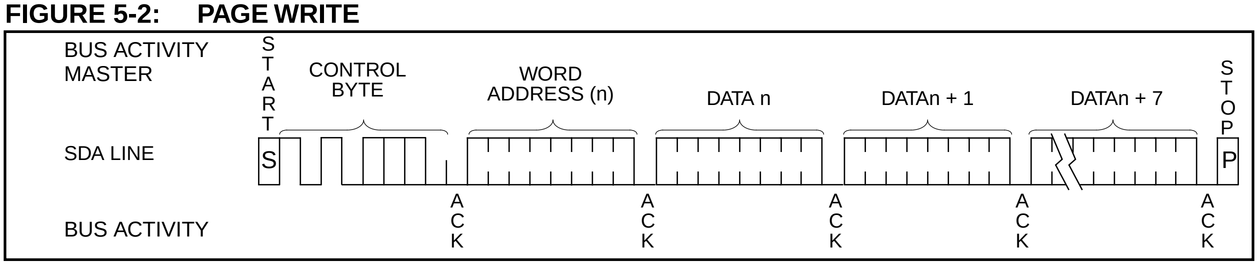


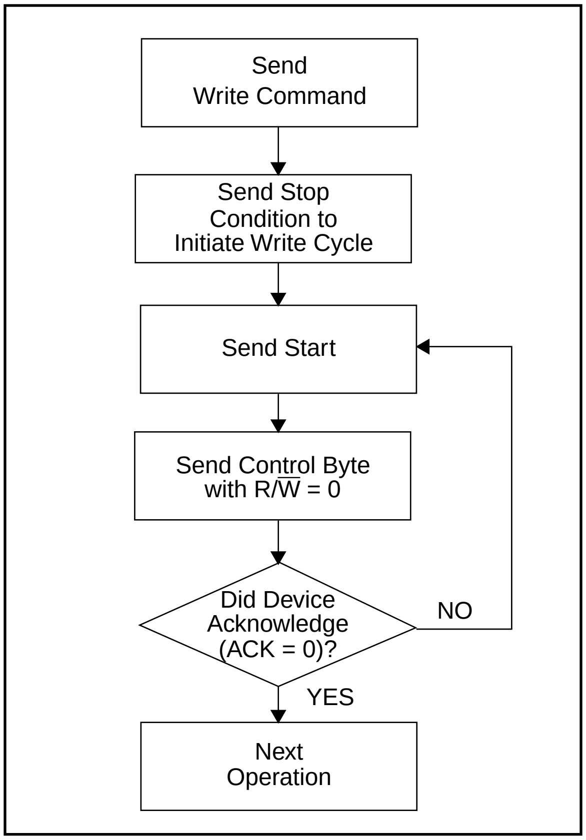
FIGURE 5-2: PAGE WRITE



6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command ($R/\overline{W} = 0$). If the device is still busy with the write cycle, then NO ACK will be returned. If the cycle is complete, then the device will return the ACK, and the master can then proceed with the next read or write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



7.0 READ OPERATION

Read operations are initiated in the same way as write operations with the exception that the $R/\overline{W}$ bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

7.1 Current Address Read

The 24LC01B/02B contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with $R/\overline{W}$ bit set to one, the 24LC01B/02B issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC01B/02B discontinues transmission (Figure 7-1).

7.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24LC01B/02B as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then, the master issues the control byte again but with the $R/\overline{W}$ bit set to a one. The 24LC01B/02B will then issue an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a stop condition and the 24LC01B/02B discontinues transmission (Figure 7-1).

7.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24LC01B/02B transmits the first data byte, the master issues an acknowledge as opposed to a stop condition in a random read. This directs the 24LC01B/02B to transmit the next sequentially addressed 8-bit word (Figure 7-2).

To provide sequential reads the 24LC01B/02B contains an internal address pointer which is incremented by one at the completion of each operation. This address pointer allows the entire memory contents to be serially read during one operation.

7.4 Noise Protection

The 24LC01B/02B employs a V_{CC} threshold detector circuit which disables the internal erase/write logic if the V_{CC} is below 1.5 volts at nominal conditions.

The SCL and SDA inputs have Schmitt trigger and filter circuits which suppress noise spikes to assure proper device operation even on a noisy bus.

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FIGURE 7-1: CURRENT ADDRESS READ

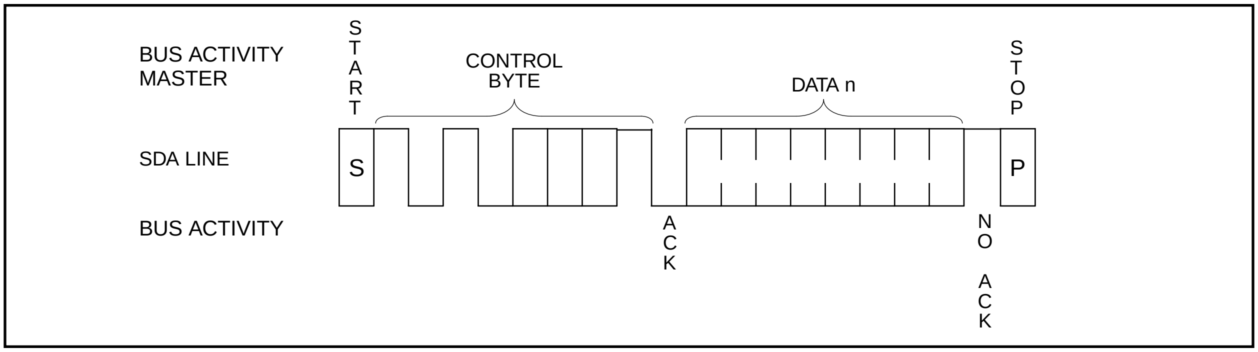


FIGURE 7-1: RANDOM READ

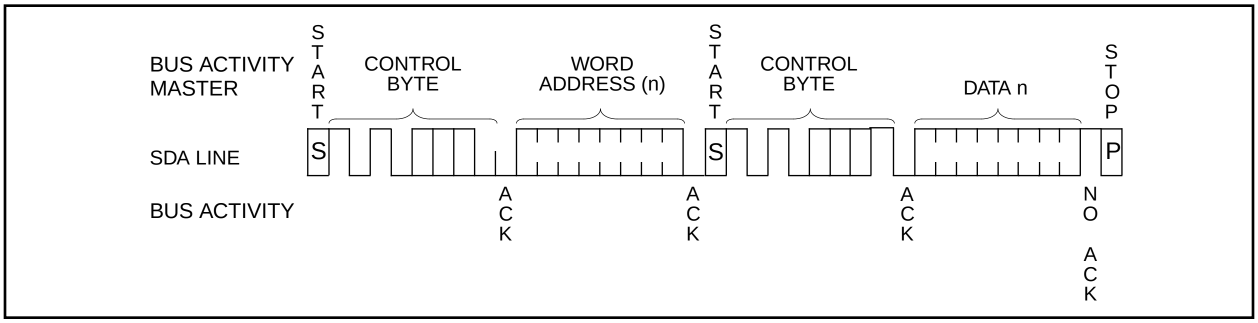
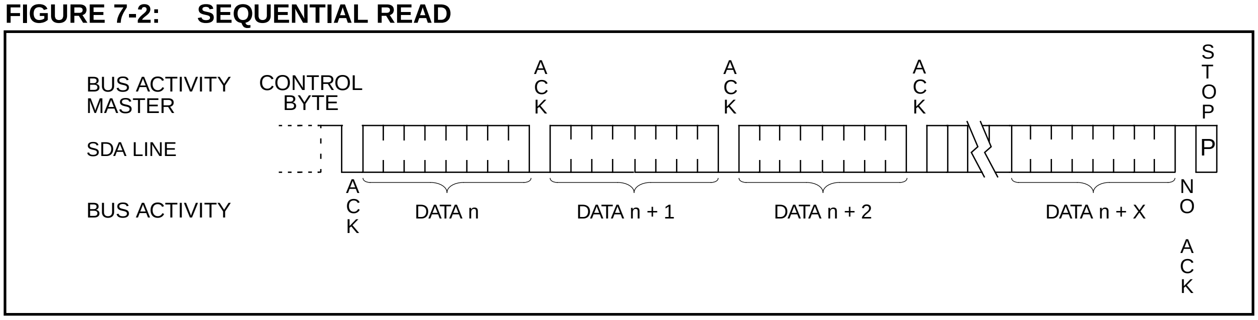


FIGURE 7-2: SEQUENTIAL READ



8.0 SHIPPING METHOD

The micromodules will be shipped to customers in clear plastic trays. Each tray holds 150 modules, and the trays can be stacked in a manner similar to shipping die in waffle packs. A tray drawing with dimensions is shown in Figure 8-1.

FIGURE 8-1: TRAY DIMENSIONS

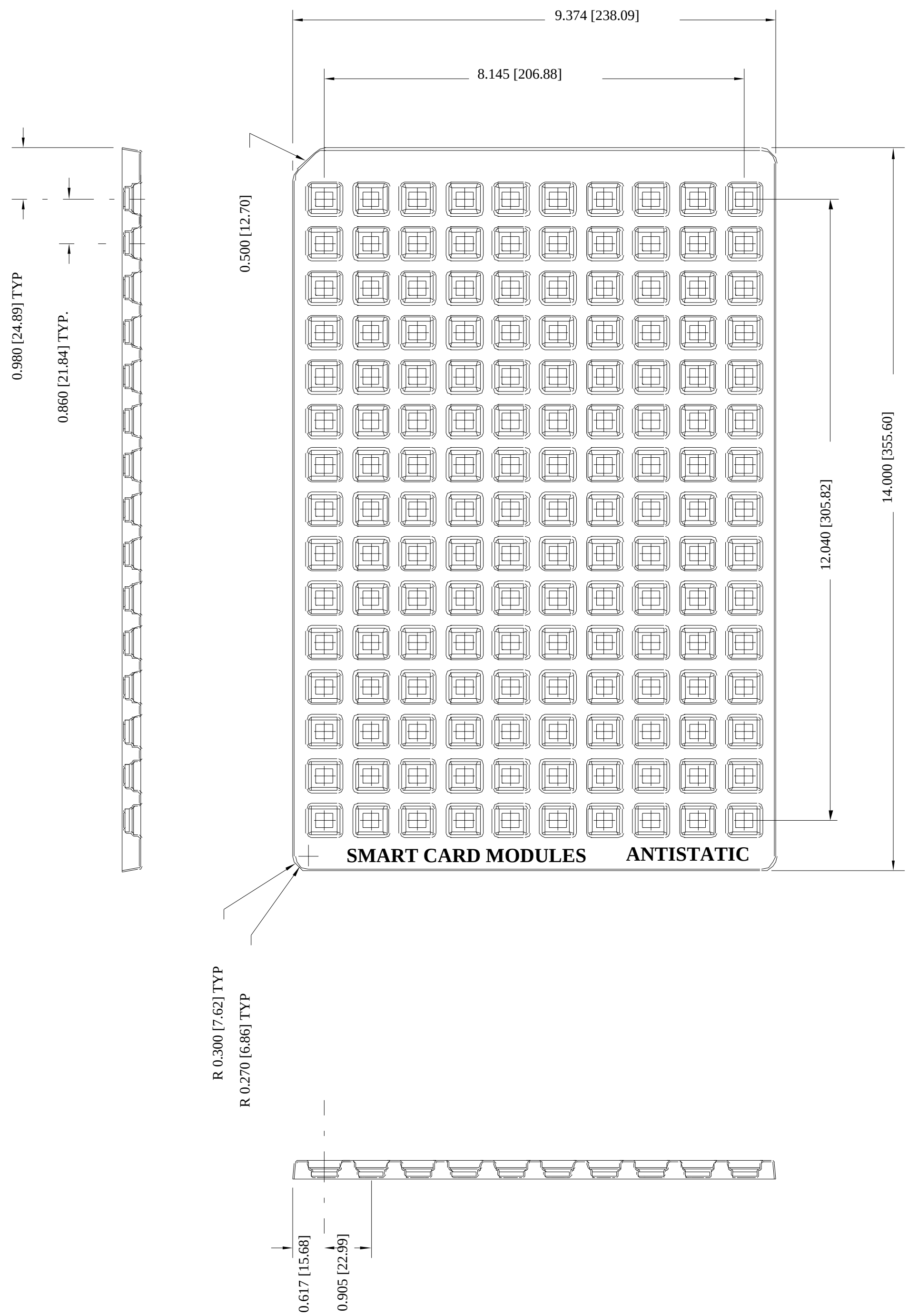


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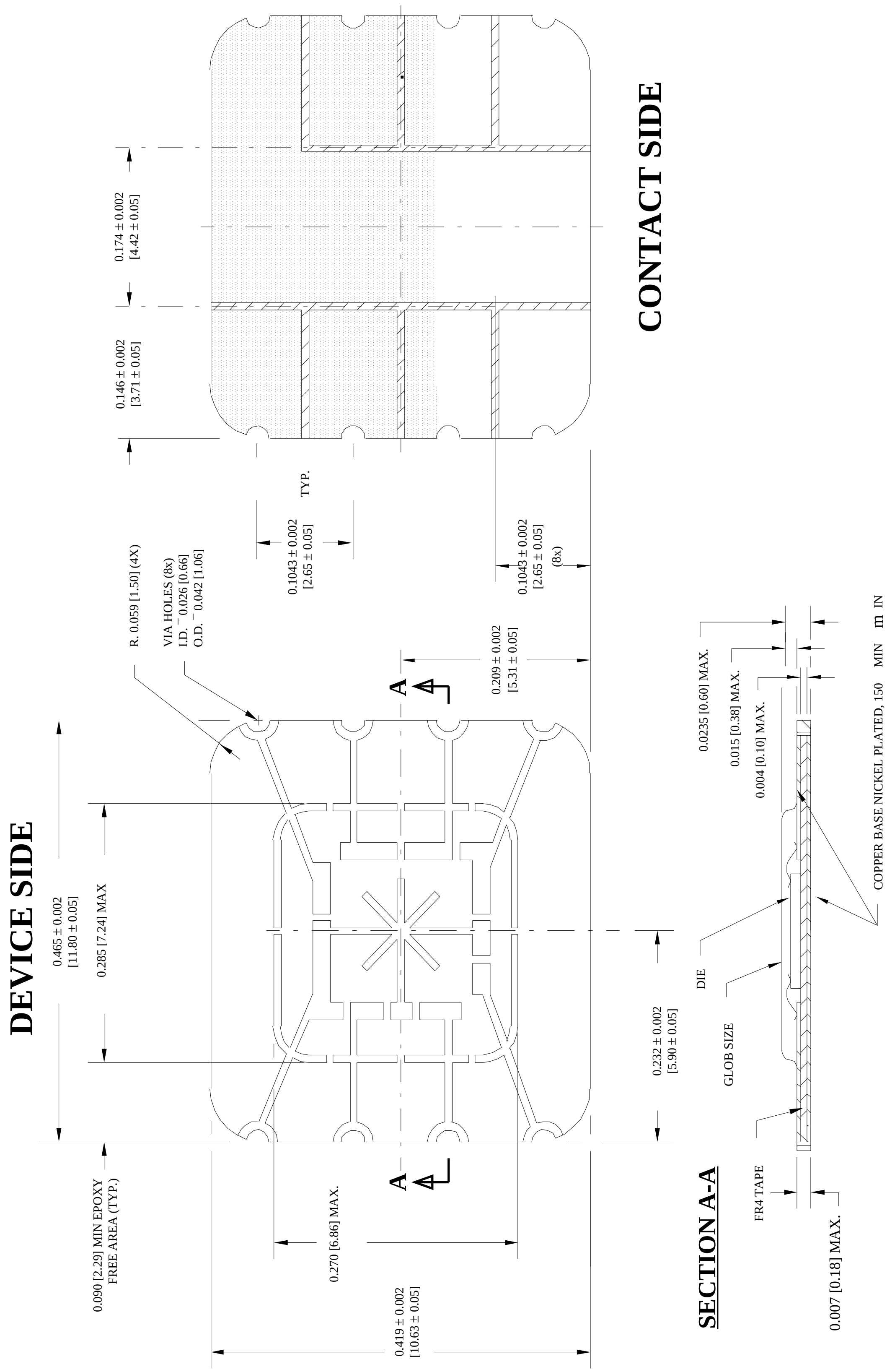
FIGURE 8-2: MODULE DIMENSIONS



NOTES:

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24LC01B/02B PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

24LC01B/02B — _ /MT

Package	MT =	Micromodules in trays
Temperature Range:	Blank =	0˚C to +70˚C
Device:	24LC01B	1K I^2C Serial EEPROM in ISO Module
	24LC02B	2K I^2C Serial EEPROM in ISO Module

Sales and Support

Data Sheets
Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

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